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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,440	03/18/2005	Kazuhiro Fujikawa	4858	4308
21553 7590 04/30/2007 FASSE PATENT ATTORNEYS, P.A. P.O. BOX 726 HAMPDEN, ME 04444-0726			EXAMINER LE, THAO P	
			ART UNIT	PAPER NUMBER
			2818	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/30/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/528,440

Applicant(s)

FUJIKAWA ET AL.

Examiner

Thao P. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,6-11 and 25-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,6-8, 10-11 and 25-27,29 is/are rejected.
- 7) ☒ Claim(s) 9,28 and 30-32 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Amendment

This office action is responsive to communication(s) filed on 01/16/2007.

Claims 1, 6-11, 25-32 are pending, including new additional claims 27-32.

Claims 1, 6-7, 9-11, 25-26 have been amended.

Claims 2-5, 12-24 have been cancelled.

Remarks of applicants have been fully considered but the arguments are not found persuasive. Applicant's arguments (see pages 8-10 of Remarks) are not found persuasive. Cited references do not disclose the use of SiC substrate, however, the use of SiC substrate is conventional, as described in applicant's background, that SiC substrate has been used in diode, FET, JFET, CMOS, or the like. In response to applicant's argument that there is no suggestion to combine the references (remarks, pages 10-11), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In page 12 of Remarks, applicant stated that "a person of ordinary skill in the art would not have expected to successfully apply the teaching of JP's 120 (using polyimide resin as a mask for ion implanting) to a substrate comprising SiC semiconductor material". If using polyimide resin as a mask for ion implanting (as disclosed in JP's 120) into the SiC substrate is

unsuccessful then why applicants invent that method? (see claim 1). The method disclosed in Claim 1 of present invention is clearly the same as the method of JP's 120 applied on the SiC substrate. In response to arguments regarding the temperature required for the substrate to be at least 300 or 500 degrees, the requirement of temperature for the substrate have been stated "background art" in pages 2-4 of the specification, and it is obvious that the requirement of such temperature has been well known in the art. Applicant has not stated else where that the semiconductor substrate is heated at temperature of at least 300 or 500 degrees for ions implanted is newly invented by applicants. In fact, it is well known in the art that the SiC substrate is heated to at least 300 or 500 degrees during the ions implantation in order for ions bombardment was carried out, and also for activation and diffusion of ions were carried out. For example, U.S. Patent Nos. 629444, 6670688, 7195996, and U.S. Publication Nos. 20030040136, 20020179910, 20010046757, and other references cited in PTO-892 also disclose the method of ion implanting into the SiC substrate including the step of heating the substrate to the temperature of around 800 to thousands and some hundred degrees during the ion implantation process.

Similar responses are applied for newly added claims 27-29.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 6-7, 10-11, 25-27 are rejected under 35 USC 103 (a) as being anticipated by Japan Publication No. 04-002120 (submitted by IDS), in view of AAPA (Applicant Admitted Prior Art).

Regarding claims 1, 6-7, 27, Japan Publication No. 04-002120 discloses a method of fabricating a semiconductor device by employing ion implantation to provide a semiconductor substrate 1 at a surface thereof with a region having dopant introduced therein, comprising the steps of: providing the substrate 1 at a surface thereof with a mask layer 2 including a polyimide resin film 2, and implanting dopant ions into the substrate (Constitution). Japan Publication No. 04-002120's abstract doesn't mention that the substrate is SiC. It is well known in the art that SiC is used in the method of forming the devices such as MOS or FET in Japan Publication No. 04-002120. AAPA discloses the use of SiC layer as substrate (Page 1 of Specification). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use SiC as a substrate material because SiC material has wide band gap, large insulating electric field.

Still regarding claims 6-7, 27, Japan Publication No. 04-002120 fails to disclose the substrate is heated to at least 300 oC or 500 oC for dopant ions are implanted. However, it would have been well know in the art that the high temperature of about 800 to thousand and some hundreds degrees are used to heat the SiC substrate during the ion implantation. In addition, the selection of such parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in combination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955). See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sola* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

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Regarding claims 10-11, Japan Publication No. 04-002120's abstract doesn't mention the thin metal film or SiO₂ is posed between the polyimide and the substrate. However, AAPA states that metal layer or SiO₂ layer is formed on top of the substrate as a mask in the ion implantation process (Pages 2-3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a metal thin film or SiO₂ layer between the substrate and the polyimide in order to ensure high energy implantation in an environment of high temperature (page 3).

Regarding claims 25-26, Japan Publication No. 04-002120 discloses the mask layer is deposited on the substrate at a region to be undoped with dopant ions and the dopant ions are implanted into a region unmasked by the mask layer (the ions are doped into the regions beside the unmasked region).

Claim 29 is rejected under 35 USC 103 (a) as being anticipated by Japan Publication No. 04-002120 (submitted by IDS), in view of AAPA (Applicant Admitted Prior Art), and further in view of Lee, U.S. Patent No. 6,458,683.

Regarding claim 29, Japan Publication No. 04-002120 doesn't mention about using the wet etching to etch the polyimide resin. Lee discloses etching the polyimide material by wet etching process using HF acid. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use wet etching using HF acid to etch the polyimide resin material because the wet etching process is controllable since the etch rate of the polyimide resin is different than the etch rate of the other layers underlying the polyimide resin (SiO and SiC) and chemical used in wet

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etching is not only used as etchant but also used as cleaning chemical during the etching process.

Claim 8 is rejected under 35 USC 103 (a) as being anticipated by Japan Publication No. 04-002120 (submitted by IDS), in view of AAPA (Applicant Admitted Prior Art), and further in view of Shinagawa, U.S. Patent No. 5,628,871.

Regarding claim 8, Shinagawa discloses a method of fabricating a semiconductor device by employing ion implantation to provide a semiconductor substrate 15 at a surface thereof with a region having dopant introduced therein, comprising the steps of: providing the substrate 15 at a surface thereof with a mask layer 32 including a polyimide resin film 32, and implanting dopant ions into the substrate (abstract, Fig. 3B), wherein the polyimide resin film is formed of photosensitive polyimide resin (abstract). It would have been well known in the art that the polyimide resin film made of photosensitive polyimide resin would improve light detection.

Allowable Subject Matter

Claims 9, 28, 30-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 9 and 30 would be allowed since none of prior art teach or suggest claimed limitations of claims 1 and 27

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and wherein the polyimide resin film in claims 1 and 27 has a thickness of at least twice a depth of the doped region. Claim 28 would be allowed since none of prior art teach or suggest claimed limitations of claim 27 and wherein said step b) does not involve photolithography employing a photoresist, and wherein said method does not involve chemical vapor deposition and does not involve dry etching.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Inoue et al., U.S. Patent No. 6,700,631, discloses a method of forming a polyimide resin film as a mask layer (170, Fig. 12) on the SiC substrate and implanting ions into the substrate.

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ' 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire **THREE MONTHS** from the date of this action. In the event a first response is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and

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any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1785. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on 571-272-1907. Other inquiries of this application should be called to (571) 272-1562 or the fax number (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le
Primary Examiner
April 17, 2007.